Amendments to the Claims

1-13. (Canceled).

14. (Previously Amended) A self aligned source of a flash memory cell on a substrate, the self aligned source comprising:

horizontal surfaces planar to the substrate having a first doping concentration;

vertical surfaces coupled to the horizontal surfaces, said horizontal and vertical surfaces together defining a trench, wherein the vertical surfaces have a second doping concentration lower than said first doping concentration; and

a deposited vertical phosphorous-doped oxide layer provided only on the vertical surfaces, the vertical phosphorous-doped oxide layer having a third doping concentration, said self-align source having a source resistance less than a similarly doped self aligned source without the vertical phosphorous-doped oxide layer due to a more uniformed doping concentration throughout the self aligned source.

15. (Previously Presented) The self aligned source of claim 14, wherein the third doping concentration and the second doping concentration produce an effective doping concentration substantially equal to the first doping concentration..

16. (Previously Presented) The self aligned source of claim 14, wherein the third doping concentration is selected from a range from about 1% to about 6%.

17. (Previously Amended) The self aligned source of claim 14, wherein the vertical phosphorous-doped oxide layer has a thickness selected from a range of about 25Å to about 500Å.

18. (Currently Amended) The self aligned source of claim 14, wherein the third doping concentration and a thickness of the vertical phosphorous-doped oxide layer are selected to achieve desired characteristics of the flash memory cell, said desired characteristics include program rate, ~~ease~~erase rate, and data retention.

19-21. (Canceled).

22. (New) The self aligned source of claim 14, further comprising a re-oxidation oxide provided over the vertical surfaces with the vertical phosphorous-doped oxide layer and the horizontal surfaces.

23. (New) The self aligned source of claim 14, wherein the substrate is silicon.

24. (New) The self aligned source of claim 14, wherein the flash memory cell further comprises a field isolation oxide provided in the trench.

25. (New) The self aligned source of claim 14, wherein the flash memory cell further comprises a field isolation oxide provided in the trench over the vertical surfaces with the vertical phosphorous-doped oxide layer and the horizontal surfaces; a floating gate provided over said

horizontal surfaces; a polysilicon layer provided over said floating gate; and a second deposited vertical phosphorous-doped oxide layer provided on vertical surfaces of said field isolation oxide, said floating gate, and said polysilicon layer.

26. (New) The self aligned source of claim 14, wherein the flash memory cell further comprises a field isolation oxide provided in the trench over the vertical surfaces with the vertical phosphorous-doped oxide layer and the horizontal surfaces; a tunnel oxide layer provided over at least one of said horizontal surfaces; a floating gate provided over said tunnel oxide layer; an oxide-nitride-oxide (ONO) layer provided over said floating gate; a wordline polysilicon layer provided over said ONO layer; and a second deposited vertical phosphorous-doped oxide layer provided on vertical surfaces of said field isolation oxide, said tunnel oxide layer, said floating gate, said ONO layer, and said polysilicon layer.

27. (New) The self aligned source of claim 14, wherein the flash memory cell is selected from EPROM and EEPROM type memory cells.

28. (New) The self aligned source of claim 14, wherein the flash memory cell is provided in a computer system.